IN THE CLAIMS

The following claim listing is intended to reflect amendment of previously pending claims 41, 43-45, 47, 49-52, 55, 61-62, 67, 72-74, and 77. Claims 41-77 remain pending in the present application.

The specific amendments to individual claims are detailed below.

1. - 40. (Canceled)

41. (Currently Amended) A circuit on a single substrate, comprising:

a logic ~~device~~ circuit portion, wherein the logic ~~device~~ circuit portion further includes a transistor with a dielectric layer having a first thickness including a top layer which exhibits ~~a high~~ higher resistance to oxidation ~~at high temperatures~~ than the substrate material; and

a memory ~~device~~ circuit portion coupled to the logic ~~device~~ circuit portion, wherein the memory ~~device~~ circuit portion further includes a transistor with a dielectric layer having a second thickness greater than the dielectric layer of the first thickness but less than 12 nanometers, wherein the dielectric layer of the second thickness is formed entirely of silicon dioxide (SiO2).

42. (Original) The circuit of claim 41, wherein the dielectric layer having a first thickness includes a dielectric layer of less than 7 nanometers, wherein the dielectric layer has a bottom layer of silicon dioxide (SiO2), and wherein the top layer is silicon nitride (Si3N4).

43. (Currently Amended) The circuit of claim 41, wherein the logic ~~device~~ circuit portion transistor and the memory ~~device~~ circuit portion transistor both include a gate formed from boron doped polysilicon, and wherein the top layer of the dielectric layer having a first thickness exhibits a ~~strong~~ higher resistance to boron penetration ~~at high temperatures~~ than silicon dioxide.

44. (Currently Amended) The circuit of claim 43, wherein the top layer of the dielectric layer having a first thickness exhibits ~~a strong~~ resistance to boron penetration at temperatures above approximately 300 degrees Celsius.

45. (Currently Amended) The circuit of claim 41, wherein the dielectric layer of a first thickness ~~having a top layer which exhibits a high resistance to oxidation at high temperatures~~ includes a top layer of silicon nitride (Si3N4) which comprises approximately a third of the first thickness of the dielectric layer.

46. (Original) The circuit of claim 45, wherein the top layer of the dielectric layer of the first thickness has a thickness of less than 2 nanometers.

47. (Currently Amended) A system on a chip, comprising:

a logic ~~device~~ circuit portion, wherein the logic ~~device~~ circuit portion further includes a transistor with a dielectric layer having a first thickness of less than 7 nanometers including a top layer which exhibits ~~a high~~ higher resistance to oxidation ~~at high temperatures~~ than the substrate material; and

a memory ~~device~~ circuit portion coupled to the logic ~~device~~ circuit portion, wherein the memory ~~device~~ circuit portion further includes a transistor with a dielectric layer having a second thickness greater than the dielectric layer of the first thickness but less than 12 nanometers.

48. (Original) The system of claim 47, wherein the dielectric layer having a first thickness includes a dielectric layer having a bottom layer of silicon dioxide (SiO2), and wherein the top layer is silicon nitride (Si3N4).

49. (Currently Amended) The system of claim 47, wherein the logic ~~device~~ circuit portion transistor and the memory ~~device~~ circuit portion transistor both include a gate formed from boron doped polysilicon, and wherein the top layer of the dielectric layer having a first thickness exhibits a strong resistance to boron penetration at high temperatures.

50. (Currently Amended) The system of claim 49, wherein the top layer of the dielectric layer having a first thickness exhibits ~~a strong~~ resistance to boron penetration at temperatures above approximately 300 degrees Celsius.

51. (Currently Amended) The system of claim 49, wherein the top layer of the dielectric layer having a first thickness exhibits ~~a strong~~ resistance to boron penetration at temperatures above approximately 800 degrees Celsius.

52. (Currently Amended) The system of claim 47, wherein the dielectric layer of a first thickness ~~having a top layer which exhibits a high resistance to oxidation at high temperatures~~ includes a top layer of silicon nitride (Si3N4) which comprises approximately a third of the first thickness of the dielectric layer.

53. (Original) The circuit of claim 52, wherein the top layer of the dielectric layer of the first thickness has a thickness of less than 2 nanometers.

54. (Original) The system of claim 52, wherein the dielectric layer of the second thickness is formed entirely of silicon dioxide (SiO2)

55. (Currently Amended) A circuit on a single substrate, comprising:

a logic ~~device~~ circuit portion, wherein the logic ~~device~~ circuit portion includes a transistor with a dielectric layer including:

a first dielectric layer of a first thickness less than 5 nanometers;

a top layer which exhibits ~~a high~~ higher resistance to oxidation ~~at high temperatures~~ than the substrate material; and

a memory ~~device~~ circuit portion coupled to the logic ~~device~~ circuit portion, wherein the memory ~~device~~ circuit portion further includes a transistor with a second dielectric layer having a second thickness greater than the dielectric layer of the first thickness.

56. (Previously Presented) The circuit of claim 55, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

57. (Previously Presented) The circuit of claim 55, wherein first dielectric layer of a first thickness includes silicon dioxide (SiO2) and the top layer includes silicon nitride (Si3N4).

58. (Previously Presented) The circuit of claim 55, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO2).

59. (Previously Presented) The circuit of claim 55, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

60. (Previously Presented) The circuit of claim 55, wherein the top layer includes a top layer of silicon nitride (Si3N4) which comprises approximately a third of the first thickness of the first dielectric layer.

61. (Currently Amended) The circuit of claim 55, wherein the top layer exhibits ~~a high~~ higher resistance to boron penetration ~~at high temperatures~~ than silicon dioxide.

62. (Currently Amended) A circuit on a single substrate, comprising:

a logic ~~device~~ circuit portion, wherein the logic ~~device~~ circuit portion includes a transistor with a dielectric layer including:

a first dielectric layer of a first thickness less than 5 nanometers;

a top layer which exhibits ~~a high~~ higher resistance to boron penetration ~~at high temperatures~~ than silicon dioxide; and

a memory ~~device~~ circuit portion coupled to the logic ~~device~~ circuit portion, wherein the memory ~~device~~ circuit portion further includes a transistor with a second dielectric layer having a second thickness greater than the dielectric layer of the first thickness.

63. (Previously Presented) The circuit of claim 62, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

64. (Previously Presented) The circuit of claim 62, wherein first dielectric layer of a first thickness includes silicon dioxide (SiO2) and the top layer includes silicon nitride (Si3N4).

65. (Previously Presented) The circuit of claim 62, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO2).

66. (Previously Presented) The circuit of claim 62, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

67. (Currently Amended) A circuit on a single substrate, comprising:

a logic ~~device~~ circuit portion, wherein the logic ~~device~~ circuit portion includes a transistor with a dielectric layer including:

a first dielectric layer of a first thickness less than 5 nanometers;

a silicon nitride (Si3N4) top layer ~~which exhibits a high resistance to oxidation at high temperatures~~; and

a memory ~~device~~ circuit portion coupled to the logic ~~device~~ circuit portion, wherein the memory ~~device~~ circuit portion further includes a transistor with a second dielectric layer having a second thickness greater than the dielectric layer of the first thickness.

68. (Previously Presented) The circuit of claim 67, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

69. (Previously Presented) The circuit of claim 67, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO2).

70. (Previously Presented) The circuit of claim 67, wherein the second dielectric layer of a second thickness includes a dielectric layer having a thickness of less than 12 nanometers.

71. (Previously Presented) The circuit of claim 67, wherein the silicon nitride (Si3N4) top layer includes a silicon nitride (Si3N4) top layer with a thickness of approximately a third of the first thickness of the first dielectric layer.

72. (Currently Amended) The circuit of claim 67, wherein the top layer ~~exhibits a high resistance to boron penetration at high temperatures~~ has a thickness of less than 2 nanometers.

73. (Currently Amended) A circuit on a single substrate, comprising:

a logic ~~device~~ circuit portion, wherein the logic ~~device~~ circuit portion includes a transistor with a dielectric layer including:

a first dielectric layer of a first thickness less than 5 nanometers;

a silicon nitride (Si3N4) top layer of approximately a third of the first thickness ~~which exhibits a high resistance to oxidation at high temperatures~~; and

a memory ~~device~~ circuit portion coupled to the logic ~~device~~ circuit portion, wherein the memory ~~device~~ circuit portion further includes a transistor with a second dielectric layer having a second thickness of less than 12 nanometers (nm).

74. (Currently Amended) The structure of claim 73, wherein the top layer ~~exhibits a high resistance to boron penetration at high temperatures~~ has a thickness of less than 2 nanometers.

75. (Previously Presented) The structure of claim 73, wherein the first dielectric layer and the top layer together have a thickness of less than 7 nanometers (nm).

76. (Previously Presented) The structure of claim 73, wherein the second dielectric layer of a second thickness includes a dielectric layer formed entirely of silicon dioxide (SiO2).

77. (Currently Amended) A circuit on a single substrate formed by the method comprising:

forming a logic ~~device~~ circuit portion including a first transistor and a memory ~~device~~ circuit portion including a second transistor on a single substrate;

forming a pair of gate oxides on the first transistor and the second transistor to a first thickness of less than 5 nanometers (nm) by krypton plasma generated atomic oxygen at less than or equal to approximately 400 degrees Celsius;

forming a thin dielectric layer on one of the pair of gate oxides, wherein the thin dielectric layer exhibits higher resistance to oxidation ~~at high temperatures~~ than the substrate material; and

forming the other of the pair of gate oxides to a second thickness.

Respectfully Submitted,

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